Reliability Challenges and Design Considerations for Wafer-Level Packages

Xuejun Fan[1,2], Qiang Han[1]
Department of Engineering Mechanics

2008 International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP 2008)
978-1-4244-2740-6/08/$25.00 © 2008 IEEE

Cu Post WLP

Fig. 2 shows a schematic of Cu post WLP structure. The processes involving in making the Cu post is shown in Fig. 3 [6], peripheral pads on the wafer are rearranged in a real array pattern after photolithographic plating. Then metal posts about 100μm high are fabricated on the wafer. After encapsulating the entire surface of the wafer using the new encapsulation method, a package the same size as the chip is fabricated using a wafer-level packaging method. This method involves dividing the wafer into individual semiconductor packages by a standard dicing process. The detailed processes are described in the following,

1. The first step in the formation of posts and the rearrangement of pads is the formation of a polyimide cover film on a device wafer. This layer is a stress buffer against molding pressure. It also improves the adhesive properties between the wafer and the encapsulant. In the next step, the sputtering is applied to fabricate a thin metal film onto the surface of the wafer. The film consists of an adhesion metal layer and a conducting layer (copper in general). These thin metal films are the plating base used in the rerouting process and the metal post-forming process. After forming a patterned resist on the thin metal film surface, a redistribution trace is fabricated by electrolytic plating. After these processes, the resist is reformed and posts are formed by electrolytic plating. Finally, the resist is peeled off, the sputtered film is etched and the post-forming process is completed.

2. The mold die is divided into two pieces, an upper and a lower die. The lower die consists of inner and outer dies. These mold dies are heated to approximately 175 C and a temporary film is held by vacuum to upper die. The wafer on which the posts are formed is set on the inner die of the lower die and an encapsulant tablet is placed on the central part of the wafer with metal posts. The temporary film has three functions. To prevent the encapsulant from making contact with the upper die. 2) To disperse the mold pressure over the entire surface of the wafer. 3) To expose the top of the posts in the next stage. When clamping the mold die, the encapsulant tablet melts by applying heat and pressure. The encapsulant spreads over the entire wafer surface and hardens by held inside the mold die. Even though the encapsulant leaving out mold release agent and has an extremely high adhesive force, the encapsulated wafer can be released easily. This is because only a peripheral part of the mold die comes in contact with the encapsulant.

   Table 1 showed the reliability test results of a Cu post WLP package[6]. It clearly indicated that the reliability performance has been improved greatly.

BOP WLPs, the bump rests on the polymer, and thus any stress applied to the solder bump directly propagates to the underlying polymer. The polymer must be designed to ensure sufficient mechanical toughness and adhesion to adjacent materials to qualify for the BOP structure.

The fabrication steps shown in Fig 5 follow the typical application steps used with photo definable polyimides [3]. The process is straightforward and requires two masks for opening vias in the dielectric layers and two masks for the metallization. The chosen polymer is photosensitive and positive acting, as are most photoresists in use today. Starting from a customer supplied wafer, a layer of polymer is applied

10. Elenius P. The Ultra CSP wafer level package. In: 4th Pan Pacific Microelectronics Symposium, February 1999.
11. Yang H, Elenius P, Barrett S, Schneider C, Leal J, Moraca, R, et al. Reliability characterization in ultra CSP package development. In: IEEE 50th ECTC, Las Vegas, Nevada, 21–24 May 2000.
12. Reche JJH. High density multichip interconnect and packaging technology. In: IEEE IEMT Workshop on Multichip Interconnection, Orlando, FL, 10–13 October 1988.
13. Kim D-H, Elenius P, Johnson M, Barrett S. Solder joint reliability of a polymer reinforced wafer level package, Microelectron Reliab 2002;42:1837;
14. W. Eaglemier, “Achieving solder joint reliability in a lead-free world”,
15. Okinaga, N.; Kuroda, H.; Nagai, Y., “Excellent reliability of solder ball made of a compliant plasticcore”, Electronic Components and Technology Conference, 2001. Proceedings., 2001 Page(s):1345 - 1349